BY BONNIE BAKER

Changing the PWM signal to dc

You can generate a variable dc reference voltage with a DAC or with a PWM (pulse-width-modulation) signal from your controller (**Figure 1**). The accuracy of the voltage source that the PWM/lowpass-analog-filter combination generates is as accurate as your onboard timer, filter operational amplifier, and power-supply voltage. If your controller has 64 divisions available for the PWM function, this function's accuracy can be as low as 78 mV in a 5V system.

With a microcontroller PWM generator, the clock sets the fundamental frequency. You then adjust the duty cycle by changing the ratio of T_{ON} to T_{OFF}. T_{ON} is the high time of the PWM signal, and T_{OFF} is the low time. $T_{ON}+T_{OFF}=T$, where T is the time of one cycle (or period) from the PWM.

The number of divisions (K) that your clock can produce during the PWM period determines one part of the accuracy and granularity of your PWM reference. The highest granularity that you will get out of your adjustable voltage reference is 1/K of your full-scale range. Based on T, the number of time divisions in the period, the ideal number of bits, or the resolution, of this DAC is:

DAC resolution=log (K)/log (2) in bits.

Having an analog filter after the PWM pulse produces a dc voltage, V_{REF}. This voltage's value depends on the ratio of T_{ON} to T_{OFF} and the power-supply voltage. If the PWM signal is on more than it is off, the output voltage after the filter in an inverting configuration will be below midscale, where midscale equals $V_{DD}/2$.

If you properly filter the PWM signal on the controller's output port, the errors in this system are the quantization error from the controller clock, the I/O gate's output-swing range, the lowpass filter's ripple rejection, and any offset errors and output-swing limitations of the lowpass-filter amplifier circuit. In **Figure 1**, the FFT plot separates the PWM's square-wave response into its equivalent frequencies. **Figure 1** also shows a lowpass filter's frequency response.

The calculation of the analog filter's single-pole corner frequency for this circuit is: $f_{C(FIRST\text{-}ORDER\ FILTER)}=f_{PWM}/\sqrt{((10^{-ASTOP/20})^2-1)}$.

If you need your voltage reference to remain stable under transient conditions, you may want to increase the filter corner frequency or filter order. In this case, a higher order filter is a good alternative, because you already have an amplifier in the circuit. Designing active analog filters is easy if you use the free lowpass-filter software from various op-amp manufacturers.

With the design equations in this column, a PWM, and an op amp, you can design a DAC that generates a dc reference voltage. This design's frequency-limiting factors are the clock speed of your controller's fundamental PWM signal and the analog lowpass filter's cutoff frequency. If you want to improve this system's frequency response, you can use a faster clock without compromising the PWM/DAC, or you can use a stand-alone DAC. Using a stand-alone DAC may be attractive if your application requires precision. EDN

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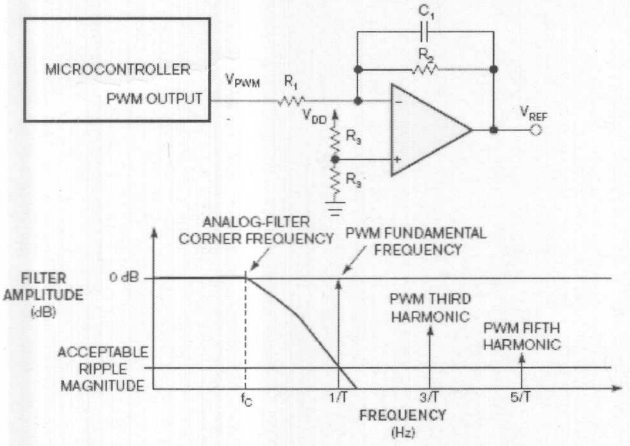

Figure 1 A hardware implementation of a PWM voltage reference uses a controller to generate the PWM signal (a). The analog, first-order, lowpass filter changes the PWM signal to a dc voltage. The primary frequency generated at the output of the PWM generator in the FFT plot is equal to 1/T, where T is the number of time divisions in the period (b). When designing the analog lowpass filter, the fundamental-frequency (f_C) response dominates the calculations and results.